Low-Voltage Broadband BiCMOS MMICs for Low-Cost High-Speed Wireless Networks Applications

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Abstract

This paper describes low-voltage BiCMOS MMICs for wireless personal communication applications. Design considerations and performance results for a developed 2V 1.6- 6.2 GHz MMIC family including bipolar-based RF amplifiers, MOS- based IF amplifiers, BiCMOS-based simplified Gilbert mixers, and downconverter as well as upconverter IC's will be presented.

Introduction

Recent popularity and demand for sophisticated cellular phone and wireless LAN systems, including 1.8 GHz GSM, 1.9 GHz PCS/DECT, 2.4 GHz IMS band WAN, and 5.2 GHz Hiperlan [1]-[3], have directed activities toward development of low- cost high- speed low- power semiconductor chips with RF to baseband frequency coverage [4]-[7]. Si technology, with continuing progress for both bipolar and CMOS devices, could be an attractive candidate for these RF frequency ranges. The BiCMOS version of a Si has been, however, so far limited to digital applications because of limited high frequency performance of MOS devices. We have initiated development of GHz-class low-power BiCMOS MMIC family including RF/IF amplifiers, mixers, and down/up converters for the front-end part of a wireless personal system, which will be described in the present paper.

Circuit Design Aspects

We have adopted an optimum combination of high frequency potential features of bipolar transistors with low power characteristics of MOS devices for different stages in each MMIC for achieving the highest performance at a supply voltage of 2V, obtaining a broadband RF frequency covering 1.6 to 6.2 GHz and a wide IF bandwidth of up to 1000 MHz, and highly suppressing unwanted signals without employing a particular filtering circuit which otherwise increase the chip size. Moreover, a high impedance inter- stage matching design method was applied for keeping the power consumption low, and avoiding gain degradation.

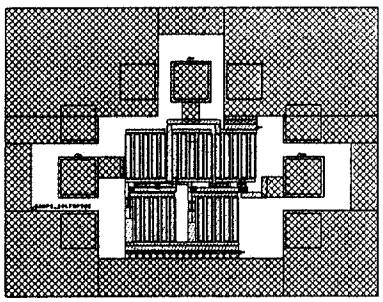

Fig. 1. Bipolar RF amplifier.

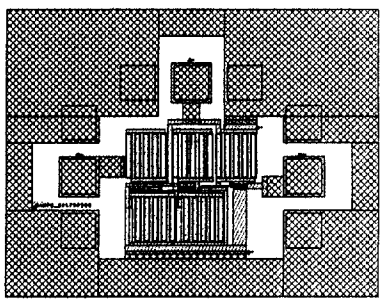

Fig. 2. NMOS IF amplifier.

To enhance a high frequency operation for the modules, a bipolar-based circuit topology was adopted for the RF amplifier which is shown in Fig. 1. The amplifier has a simple 2-stage common emitter configuration followed by an emitter follower buffer stage. The IF amplifier, shown in Fig. 2, resembles the RF amplifier but utilizes NMOS transistors which require less DC power and can provide sufficient gain for the IF signal frequency range. The IF amplifier is also responsible for attenuating high frequency components at the amplifier's output port, through an RC-filtering aspect of bias resistors and the NMOS gate-source capacitance.

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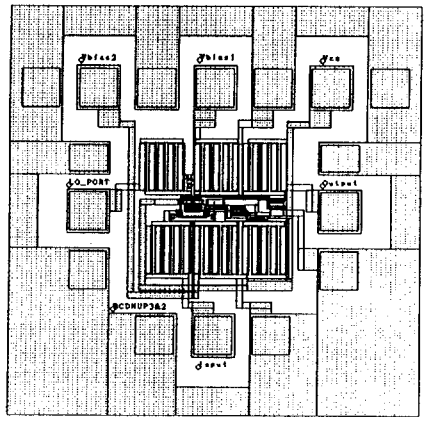


Fig. 3. BiCMOS down-mixer.

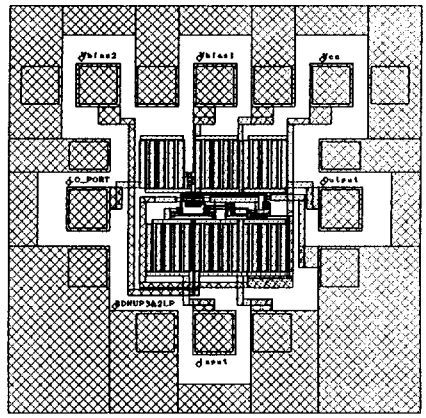


Fig. 4. BiCMOS up-mixer.

To assure a 2V DC power operation and low LO power requirement, a simplified Gilbert cell was adopted for the down- and up- mixers, and voltage drop distribution for load resistors series-gated transistors, and current source transistors in the cell was optimized. Use is made of bipolar transistors in the cell which is responsible for a high frequency mixing of the LO and RF signals. A current source circuit for each mixer employs NMOS transistors for their low power requirement and applicability as a power control device. The down-mixer, shown in Fig. 3, utilizes an NMOS push-pull buffer stage, while the up-mixer, shown in Fig. 4, uses a bipolar emitter follower buffer stage. Each downconverter and upconverter module consists of an RF amplifier, an IF amplifier, and a corresponding mixer. The present frequency converter modules make use of no particular on-chip or off-chip filter for suppressing unnecessary signals at the output port. High frequency filtering characteristics of NMOS push-pull buffer stage in the downconverter module's mixer and an optimized RC-filtering feature of the NMOS IF amplifier are utilized to realize an excellent isolation characteristics for each module.

Microwave Performance

The chips were fabricated employing a $0.4\mu m$ ECL-BiCMOS process technology which has been developed for high speed digital circuit applications [8]. The RF amplifier draws 5mA from a 2V bias supply to exhibit a small signal power gain higher than 15dB, and a noise figure lower than 4dB for a frequency of up to 4GHz, as shown in Fig. 5. The output power at 1-dB gain compression point is about 0dBm for an input signal frequency of 2.4GHz.

The IF amplifier, on the other hand, draws 3mA

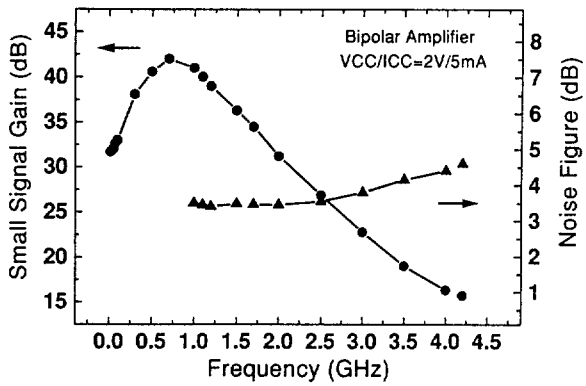


Fig. 5. RF amplifier performance.

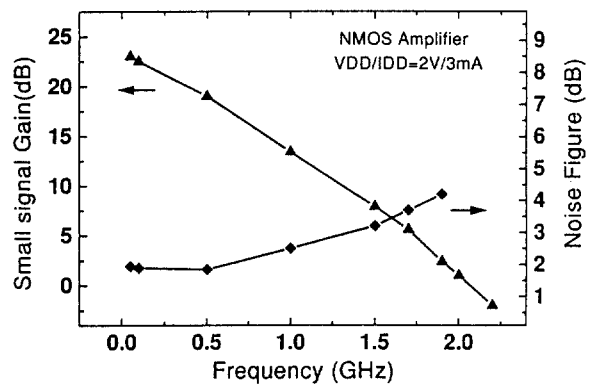


Fig. 6. IF amplifier performance.

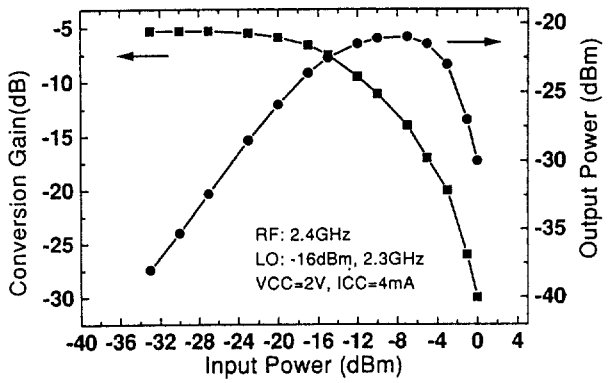


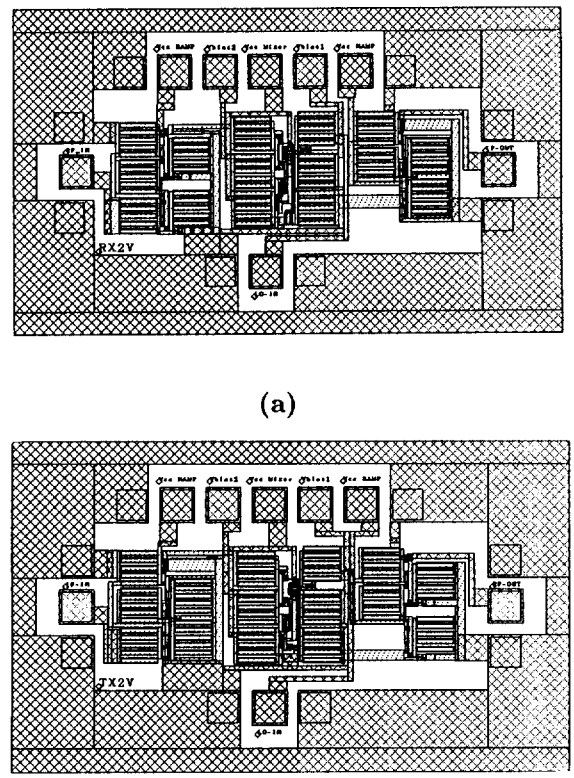
Fig. 7. Mixer performance.

from a 2V bias supply to exhibit a small signal power gain higher than 13dB, and a noise figure lower than 2.5dB for a frequency of up to 1GHz, as shown in Fig. 6. The output power at 1-dB gain compression point is about -5dBm for an input signal frequency of 400MHz. Moreover, as shown in Fig. 7, for an LO frequency and power level of 2.3GHz and -16dBm and an RF frequency of 2.4GHz, the down-mixer and up-mixer chips exhibit a small signal conversion gain of higher than -8dB, under a 2V bias condition.

Chip layout patterns for the downconverter and upconverter modules, are shown in Figs. 8(a) and 8(b), respectively. Chip size for the downconverter and upconverter modules is $1.0mm \times 0.7mm$. Performance results for the downconverter and upconverter chips versus the IF frequency, for an input power of -40dBm, an LO power of -16dBm, and the LO frequency as a parameter, are shown in Figs. 9(a) and 9(b). Each chip dissipates less than 24mW of DC power to cover the full L-S-C band with an IF frequency of several 100MHz and a sufficient conversion gain.

As shown in Fig. 10, the downconverter has a double sideband noise figure of 5.5-8.5dB over 0.5-4GHz. While the maximum conversion gain is achieved for a DC voltage of 2.05-2.10V, both chips exhibit a graceful degradation for a $\pm 0.15V$ voltage deviation. Measured LO-IF and RF-IF isolation for the downconverter are better than 30dB for an IF frequency of up to 500MHz, and better than 23dB for an IF frequency of up to 1000MHz. On the other hand, maximum LO-RF and IF-RF isolation for the upconverter are, respectively, 18dB and 14dB. 3rd order intermodulation product power levels for the downconverter and upconverter were measured to be 5dBm.

With a final target of a 25Mbps dual - mode cellular–LAN PCMCIA card system realization, development of an experimental test-bed system has been initiated.



(a)

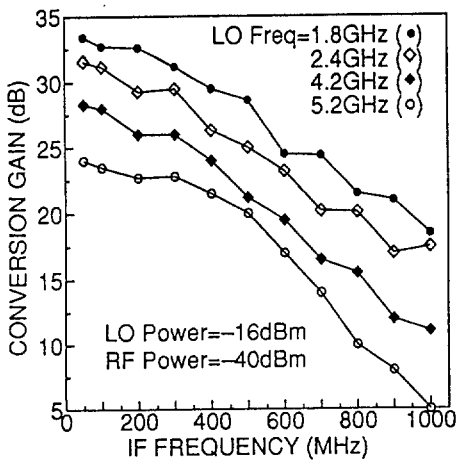
(b)

Fig. 8. Layout patterns for (a) downconverter and (b) upconverter.

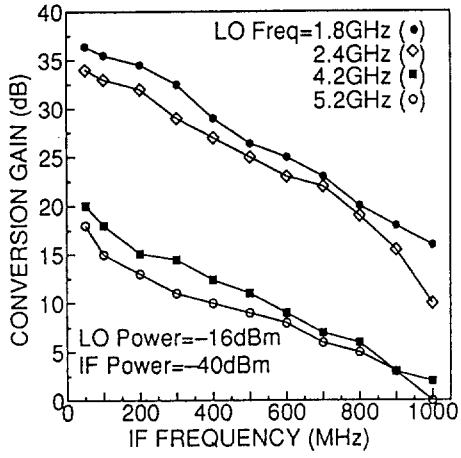
The fabricated downconverter and upconverter chips have been successfully incorporated in this experimental test-bed system. The system comprises an RF/IF board, a MODEM board, and a PCMCIA card control board. The RF/IF board incorporating these packaged chips is shown in Fig. 11.

Conclusions

BiCMOS MMIC development activities for low - voltage broadband wireless personal system applications were described. Design considerations and performance results for a recently developed 2V 1.6-6.2 GHz MMIC family were presented. Concerning the cost, wafer cost/mm^2 for the silicon-based technologies is more than 2 times lower than that for the GaAs. As a practical example of a 2.4GHz receiver chip case, it has been revealed that silicon BJT technology cost is 1/3 of the GaAs MESFET's, and silicon BiCMOS is expected to be placed in between them. BiCMOS technology, which has been mainly applied to digital LSI's so far, is expected to create new possibilities for low-cost low-voltage RF/microwave IC applications.



(a)



(b)

Fig. 9. Downconverter (a) and upconverter (b) performance versus IF frequency with LO frequency as a parameter.

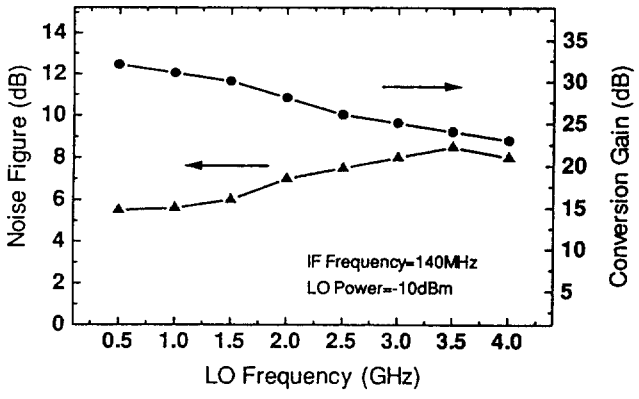


Fig. 10. Conversion gain and noise figure for the downconverter.

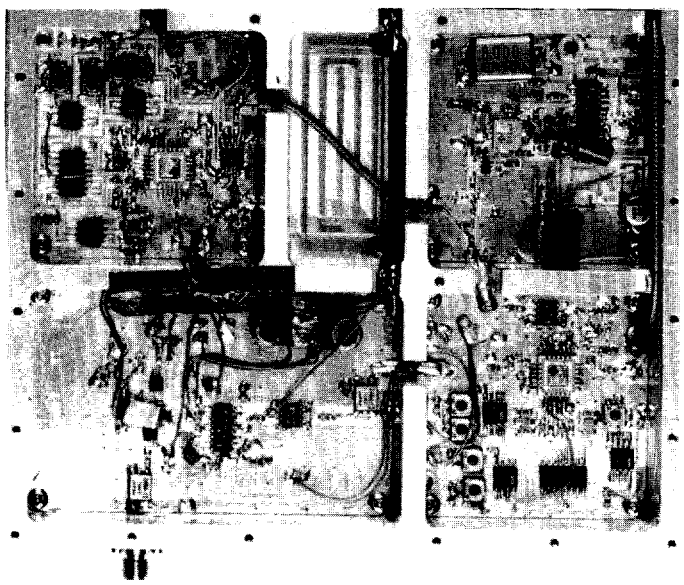


Fig. 11. RF/IF board of the PCMCIA card test-bed system.

References

[1] B. M. du Biest, "The world of GSM," GSM World Congress Digest, p. 3, Feb. 1995.

[2] J. Loraine, "Wireless data networks: an opportunity for GaAs, " GaAs IC Symp. Digest, p. 11, Oct. 1993.

[3] B. Bourin, "HIPERLAN - Markets and applications standardisation issues," Wireless Computer Networks Meeting Digest, p. 863, Sept. 1994.

[4] V. Thomas, J. Fenk, and S. Beyer, "A one-chip 2GHz single superheterodyne receiver for 2Mbps FSK radio communication," IEEE ISSCC Digest, p. 42, Feb. 1994.

[5] T. Tsukahara etal, "A 2V 2GHz Si-bipolar direct-conversion quadrature modulator," IEEE ISSCC Digest, p. 40, Feb. 1994.

[6] C. Takahashi, R. Fujimoto, S. Arai, T. Itakura, T. Ueno, H. Tsurumi, H. Tanimoto, S. Watanabe, and, K. Hirakawa, " A 1.9GHz Si direct conversion receiver IC for QPSK modulation systems," IEEE ISSCC Digest, p. 138, Feb. 1995.

[7] J. R. Long, M. A. Copeland, P. Schvan, R. A. Hadaway, "A low-voltage silicon bipolar RF front-end for PCN receiver applications," IEEE ISSCC Digest, p. 140, Feb. 1995.

[8] H. Okamura etal, "A 1ns, 1W, 2.5V, 32kb NTL-CMOS SRAM macro using a memory cell with P-channel access transistors," IEEE ISSCC Digest, p. 306, Feb. 1995.